PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-058201
(43)Date of publication of application : 03.03.1995

(51)Int.Cl. H01L 21/768
H01L 21/3205

(21)Application number : 05-202330
(22)Date of filing : 16.08.1993

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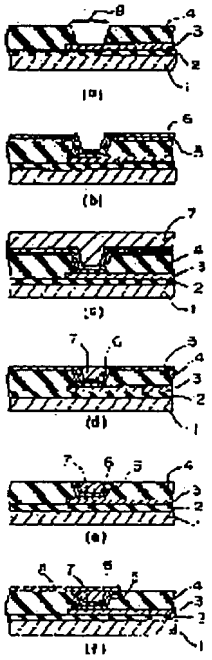
(54) MANUFACTURE OF MULTILAYER WIRING BOARD

(57)Abstract:
PURPOSE: To obtain a highly reliable multilayer wiring which can be brought into the state of high density easily by a method wherein, after a contact hole is formed in the insulating film of a board and flat surface is obtained by plating, a wiring layer is formed in such a manner that it is brought into contact with the flat surface.
CONSTITUTION: A copper thin film pattern is formed on the insulating film 2 formed on the surface of a board 1 as the first layer wiring film 3. Photosensitive polyimide is coated thereon, and after a contact hole 9, with a side of about 20μm, has been formed by conducting an exposing and developing operation, a heat treatment is conducted at 400° C for thirty minutes, and an interlayer insulating film 4 is formed. Then, after forming a titanium film 5 and a copper film 6 successively in 1μm thickness using a sputtering method, a thick copper-plating film 7 is formed on a recessed part by conducting electric plating under the condition wherein a flat surface can be obtained using the above-mentioned titanium film 5 and copper film 6 as an electrode. A titanium-copper-titanium multilayer thin film 8 is formed on the board 1 for which burying is conducted as the second wiring layer. As a result, a highly precise multilayer wiring can be obtained by reduced manhours.



LEGAL STATUS

[Date of request for examination]	14.08.2000
[Date of sending the examiner's decision of rejection]	15.10.2002
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3632981

[Date of registration]	07.01.2005
[Number of appeal against examiner's decision of rejection]	2002-021999
[Date of requesting appeal against examiner's decision of rejection]	14.11.2002
[Date of extinction of right]	

CLAIMS

[Claim(s)]
[Claim 1] The process which forms an interlayer insulation film on the 1st wiring layer formed in a substrate front face or this upper layer, and forms a contact hole in this, The process which covers said whole substrate front face with the electric conduction film, performs electroplating under conditions from which the thick plating film is obtained in a crevice, and carries out flattening of the front face by using this electric conduction film as an electrode, The process which carries out isotropic etching of said plating film so that the plating film on said interlayer insulation film may be removed and the plating film in said contact hole may be made to remain alternatively, The manufacture approach of the multilayer-interconnection substrate characterized by including the process which forms the 2nd wiring layer so that this plating film may be contacted.
[Claim 2] The process which forms the 1st interlayer insulation film on the 1st wiring layer formed in a substrate front face or this upper layer, and forms a contact hole in this, The process which besides forms the 2nd insulator layer in a layer, carries out patterning of this, removes the 2nd wiring layer pattern formation field alternatively, and forms a crevice, The process which covers said whole substrate front face with the electric conduction film, performs electroplating under conditions by which the thick plating film is formed in said crevice, and carries out flattening of the front face by using this electric conduction film as an electrode, The manufacture approach of the multilayer-interconnection substrate characterized by including the process which carries out isotropic etching of said plating film so that the plating film on said 2nd insulator layer may be removed and the plating film in said crevice may be made to remain alternatively.

[Translation done.]

* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the manufacture approach of a multilayer-interconnection substrate that started the manufacture approach of a multilayer-interconnection substrate, especially wiring was formed in high density.
[0002]
[Description of the Prior Art] In recent years, miniaturization of electronic equipment, thin-shape-izing, and high performance-ization are advanced by development of a semiconductor integrated circuit technique, and it has been an important technical problem to mount a semiconductor chip in high density on the circuit board in connection with this.
[0003] Therefore, wiring in a multilayer-interconnection substrate is also towards densification in recent years, and detailed-izing of wiring and multilayering are progressing. In order to form detailed wiring, as it is conventionally shown in drawing 5 , on the 1st-layer wiring which consists of a thin film metal layer 3 formed in substrate 1 front face through the insulating layer 2 Form a contact hole 9 to form an interlayer insulation film 4 (drawing 5 (a)), form the thin film metal layer 8 further after this (drawing 5 (b)), and a resist pattern 13 (drawing 5 (c)) is minded. The thin film metal layer 8 is etched and the method of obtaining the pattern of the 2nd-layer wiring (drawing 5 (d)) is taken.
[0004] However, since a contact hole will become still deeper if the contact hole for connecting the 2nd-layer wiring and the 3rd-layer wiring is further formed on this, since the insulator layer on a contact hole 9 serves as a concave, if it is going to form a multilayer interconnection by this approach, it becomes easy to produce the stage piece of wiring. For this reason, as shown in drawing 6 , it is necessary to shift and prepare the location of a contact hole 9 in the multilayer interconnection which forms wiring (3, 8, 13) of three or more layers, and the fall of a wiring consistency will be caused as a result.
[0005] Moreover, as a wiring layer ingredient which has the interlayer connection section, although aluminum metallurgy had been used from problems, such as adhesion with an insulating layer, and corrosion resistance, there was a problem that the resistance of aluminum was high and cost of gold was high.
[0006] For this reason, the attempt using the continuation which embedded the metal in the contact hole so that the upper part of the connection part between wiring layers might not serve as a concave is made. For example, as shown in drawing 6 , the metal membrane of thickness comparable as the insulating layer 4 formed behind is beforehand formed by vacuum deposition or the sputtering method, an insulator layer 4 is formed by the applying method on it, and the method of carrying out flattening of the front face is also proposed. However, by this approach, it is difficult to carry out flattening completely, and becomes the configuration which the metal membrane projected, and the circumference of a contact hole formed behind will rise from other parts, and will become an opposite effect on the contrary.
[0007] Moreover, although there is especially no limitation as an ingredient of this metal membrane, in order to attain the interlayer connection of low cost by low resistance, when using copper and a copper alloy, in order to prevent corrosion prevention and diffusion into an

insulator layer, the process which carries out covering protection of this upper layer after this metal membrane formation must be established, and there is a problem that a man day increases.
[0008] In order to solve such a problem, there is a selection grown method as an approach which does not need an etching process, and it is put in practical use in the production process of a semiconductor chip. This approach tends to grow up metals, such as a tungsten, only into the wiring part exposed to the contact hole pars basilaris ossis occipitalis formed into the insulator layer by chemical vapor deposition alternatively, and tends to obtain the flat interlayer connection section. However, by this approach, the metallic material to be used is limited to chemical vapor deposition and the ingredient in which selective growth is possible. Although current and the metallic material currently generally used are tungstens, it is hard to be corroded by the refractory material, and it is the ingredient which is comparatively easy to use it since there is also little diffusion to an insulator layer, it is difficult for resistivity to lower contact resistance highly. Furthermore, at a chemical vapor growth process, since substrate temperature serves as an elevated temperature comparatively, an ingredient with thermal resistance high also as an insulator layer is needed, and there is a problem that a dielectric constant will not be able to cease in an elevated-temperature process in the organic compound insulator which was highly excellent in electrical characteristics, but will be unusable inevitably.
[0009]
[Problem(s) to be Solved by the Invention] Thus, in order to realize the multilayer interconnection which has high density wiring, the interlayer connection by which flattening of the metal was embedded and carried out to the contact hole is needed. However, there was a problem that a property was good and could obtain a reliable multilayer interconnection on the occasion of densification by neither of the approaches.
[0010] This invention was made in view of said actual condition, is easy densification and aims at offering a reliable multilayer interconnection.
[0011]
[Means for Solving the Problem] Then, after forming an interlayer insulation film on the 1st wiring layer formed on the substrate and forming a contact hole in this, the electric conduction film covers the whole substrate front face in this invention, the thick plating film is formed in a crevice by using this electric conduction film as an electrode, and after performing electroplating on conditions which obtain a flat front face and performing surface flattening, the 2nd wiring layer is formed so that this plating film may be contacted.
[0012] The process which forms the 1st wiring layer on a substrate desirably, and the process which forms an insulator layer on said 1st wiring layer, and forms a contact hole in this, The process which forms the thin film conductive layer containing a refractory metal layer with the melting point higher than copper or a copper alloy on the insulator layer in which this contact hole was formed, The process which forms in said thin film conductive layer top face the thin film conductive layer which contains a refractory metal layer with the melting point higher than copper or a copper alloy using the plating bath which added the organic substance, The process which performs electroplating of copper or a copper alloy using the plating bath which added the organic substance on said thin film conductive layer top face, and carries out flattening of the substrate principal plane top by said plating film, He is trying to include the process which leaves the same thickness as said insulator layer for the copper or the copper alloy which carried out isotropic etching of said plating film, and was formed in the contact hole, and removes the plating metal membrane on a substrate principal plane.
[0013] Moreover, in the 2nd of this invention, after forming a contact hole in the 1st interlayer insulation film, in advance of formation of a thin film conductor layer, form the 2nd insulator layer, and patterning of this is carried out. Remove the 2nd wiring layer pattern formation field alternatively, form a crevice, cover the whole substrate front face with the electric conduction film after this, and this electric conduction film is used as an electrode. Perform electroplating under conditions from which the plating film thick to a crevice is obtained, and flattening of the front face is carried out. The plating film on said 2nd insulator layer is removed, it is made to carry out isotropic etching of said plating film so that the plating film in said crevice may be

made to remain alternatively, and he is trying for plating to attain the embedding of a crevice and the formation of the 2nd wiring layer resulting from a contact hole to coincidence.
[0014] The oxidation silicone film formed as said insulating layer by the polyimide resin, the applying method, the chemical vapor deposition, or the sputtering method formed by the applying method is used. He is trying to use at least one sort in titanium, nickel, vanadium, niobium, a tantalum, chromium, molybdenum, and a tungsten as a refractory metal furthermore. These are formed by vacuum deposition or the sputtering method.
[0015] In addition, it blends optimum dose every so that the level difference by which organic nitrogen compounds, an organosulfur compound, and a polyether compound are made as the organic substance added during a plating bath on the plating film front face on opening formed in the insulating layer may become as small as possible.
[0016]
[Function] According to the above-mentioned approach, it is what was made paying attention to the point that the plating film thick to a crevice is obtained and a flat front face can be obtained, for example in the case of the plating liquid using an organic additive. If it is made to end after forming a contact hole in an insulator layer, performing plating and obtaining a flat substrate front face when this plating film is etched isotropic and etching advances to the front face of an insulator layer, the plating film will be alternatively left behind only in a contact hole, and embedding will be completed. Thus, embedding is completed only by using an exposure development process only for formation of a contact hole, and the conversion error of a dimension becomes very small a top with few man days.
[0017] Flattening of a deposit film front face can be promoted by carrying out optimum dose addition of the organic substance in formation processes, such as copper by electroplating, or copper alloy film, here at a plating bath. If possible, the cathode current density in a plating process uses high current density still more preferably in the range in which burnt deposits do not occur in a deposit metal membrane, and the abnormality growth by the current concentration to a part does not take place.
[0018] In this process, by using refractory metals, such as titanium, nickel, vanadium, niobium, a tantalum, chromium, molybdenum, and a tungsten, as some cathode of electroplating, touching an insulator layer of the copper or the copper alloy by plating directly can be lost, and it can aim at the corrosion prevention of copper or a copper alloy, and the diffusion prevention to an insulator layer, and can heighten adhesive strength with an insulator layer after formation of a contact hole. In order that the organic substance may furthermore adsorb preferentially organic nitrogen compounds, an organosulfur compound, and a polyether compound on the occasion of formation of the metal membrane by electroplating compared with a crevice to the front face which is irregular by carrying out optimum dose addition by heights, a deposit of the plating film is controlled. As a result, by heights, the deposit rate of the plating film becomes slow, and since it becomes quick, when plating is continued, flattening of the front face which does not have surface irregularity as a result is carried out in a crevice. Thus, the formed metal membrane serves as uniform thickness except for the contact hole section, and, on the other hand, the contact hole section becomes thick compared with other parts. Therefore, if this film is etched using etchant whose etch rate is uniform in the thickness direction, it will leave alternatively the copper or the copper alloy inside a contact hole, and it will become possible to remove the metal membrane of other parts.
[0019]
[Example] Hereafter, it explains to a detail, referring to a drawing about the example of this invention.
[0020] First, an insulator layer 2 is formed in the front face of a substrate 1, a copper thin film pattern is formed in this upper layer as 1st-layer wiring film 3, the photosensitive polyimide by Toray Industries, Inc. by which the designation is carried out to photograph NISU UR-314 at this upper layer is applied, exposure development is performed, and it is 20 micrometers per side. The contact hole 9 of extent is formed. After this, heat treatment for about 30 minutes is performed at 400 degrees C, and an interlayer insulation film 4 is formed (drawing 1 (a)). For polyimide, the thickness after heat treatment is 20 micrometers here. The thickness at the time of spreading is

set up so that it may become extent. Moreover, in order to prevent a stage piece, exposure development conditions are controlled so that the include angle of the pars basilaris ossis occipitalis of a contact hole and a side attachment wall turns into 100 degrees or more.
[0021] Subsequently, the laminating of the titanium (Ti) film 5 and the copper (Cu) film 6 is continuously carried out one by one by the sputtering method, and the thickness as the whole is 1 micrometer. It is made to become extent. A copper film acts as plating cathode here. Moreover, titanium acts as barrier which prevents the counter diffusion of the copper which is the polyimide or the 1st-layer wiring which is a refractory metal and is an interlayer insulation film, and the plating cathode and the upper plating film. Therefore, thickness may be thin. If it is formed so that copper and polyimide may touch directly, copper will oxidize by the oxygen in polyimide, adhesion will fall, and it will become easy to exfoliate. Moreover, it forms for a titanium front face tending to oxidize continuously. Thus, the film of low resistance is formed by forming the upper film continuously, without breaking a vacuum, without the natural oxidation film intervening.
[0022] Thus, a substrate 1 is installed in an electroplating system, as shown in drawing 2 , and a copper film 6 is connected to this cathode as plating cathode. here -- as a plating bath -- a 75g [/l.] copper sulfate and sulfuric-acid (specific gravity 1.84) 100 ml/l from -- what added polyethylene-glycol 100 mg/l and thiourea 10 mg/l in the becoming solution -- using -- solution temperature -- 25 degrees C -- setting up -- current density 5 A/dm2 while stirring -- plating -- carrying out -- 20 micrometers of thickness The copper-plating film 7 of extent is formed. The level difference by the contact hole is 1 micrometer. Since it is extent, it is 20 micrometers. If the plating film of extent is formed, a front face flat enough can be obtained (drawing 1 (c)).
[0023] Then, drawing 1 (d) The copper-plating film 7 formed in substrate 1 front face is etched with the mixed solution which consists of ammonium persulfate, a sulfuric acid, and ethanol, and it removes also including the copper film 6 (plating cathode) on the front face of a substrate so that it may be shown, and you make it remain only in a contact hole.
[0024] Subsequently, drawing 1 (e) Etching removal of the titanium film 5 on substrate 1 principal plane is carried out with the etching reagent which consists of EDTA, ammonia, and hydrogen peroxide solution so that it may be shown.
[0025] Thus, the laminating thin film 8 of titanium-copper-titanium is formed in the substrate 1 which performed embedding as the 2nd wiring layer (drawing 1 (f)).
[0026] This process is repeated and you may make it form a multilayer interconnection from formation of an interlayer insulation film here if needed.
[0027] Thus, embedding is completed only by using an exposure development process for formation of a contact hole 9, there are few man days and a dimension conversion error becomes possible [performing a very small highly precise multilayer interconnection].
[0028] In addition, although said example explained the example to which direct continuation of the 1st-layer wiring and the 2nd-layer wiring was carried out, direct continuation of the 1st-layer wiring and the 2nd-layer wiring is not carried out, but one layer or other multilayer wiring layers intervene in between, and the 1st-layer wiring and the 2nd-layer wiring may be made to be connected indirectly.
[0029] Next, the resist pattern 10 is formed so that the reverse pattern of the 2nd-layer wiring may be drawn in advance of plating by this method of explaining about the 2nd example of this invention, pattern plating is performed, the crevice which removed the resist pattern 10 and was able to do it after plating is filled up with the spreading insulator layer 4, and it is characterized by performing formation of the embedding of a contact hole, and the 2nd wiring layer pattern to coincidence.
[0030] That is, it carries out like [the formation process (drawing 1 (a) and drawing 1 (b)) of plating cathode] said 1st example, and then is drawing 3 (a). The Hoechst Japan thick-film resist by which the designation is carried out to AZ-4903 so that it may be shown is applied with a spin coat method, and it is 25 micrometers of thickness. A plating-resist layer is formed and baking is performed at 90 degrees C. Then, opening of the circuit pattern of the 2nd wiring layer is carried out by exposure development, and a resist pattern 10 is obtained.
[0031] Subsequently, it installs in plating equipment like said 1st example, galvanizes on the

same conditions, and is drawing 3 (b). It is 20 micrometers of thickness so that it may be shown. The copper-plating film 7 of extent is formed. Next drawing 3 (c) An acetone removes a resist pattern 10 so that it may be shown, and the copper film 6 used as copper films other than the circuit pattern of the 2nd wiring layer formed of copper plating, i.e., plating cathode on the front face of a substrate, is etched with the mixed solution which consists of ammonium persulfate, a sulfuric acid, and ethanol. Furthermore, etching removal of the titanium film 5 on substrate 1 principal plane is carried out after this with the etching reagent which consists of EDTA, ammonia, and hydrogen peroxide solution.

[0032] Photosensitive polyimide (photograph NISU UR-3140) is applied to the substrate front face in which the 2nd wiring layer is formed after this, and the photosensitive polyimide 4 which it was formed on the 2nd wiring layer of exposure development, and has been projected is removed (drawing 3 (d)).

[0033] If photosensitive polyimide is applied again if needed after this, a still flatter front face can be obtained.

[0034] Thus, it becomes possible to obtain a multilayer interconnection easily. Drawing 3 (d) At an exposure development process, pattern precision may not be so required and a gap may produce it a little.

[0035] Moreover, drawing 3 (d) The shown exposure development process may be skipped, when flattening is fully carried out and photosensitive polyimide is applied, and an exposure development process can skip it once completely in this case.

[0036] Furthermore, what is necessary is just to make it repeat the process which applied and mentioned photosensitive polyimide above again, when forming multilayer wiring.

[0037] According to this approach, it can stop within **5% to the depth of a contact hole, and surface irregularity is 20 micrometers about the thickness of an interlayer insulation film. Or 30 micrometers Even when it carries out, surface irregularity can be stopped within **5%. It turns out that surface irregularity of this is improving sharply compared with extent of the irregularity of the front face after formation having been about **25% to the depth of a contact hole in the case of the conventional step beer method. Moreover, as a result of extent of surface irregularity decreasing sharply, it becomes unnecessary to have shifted the location of a contact hole also in the multilayer interconnection which has the wiring layer of three or more layers, the contact hole could be prepared on the contact hole, and the wiring consistency improved about 20% compared with the conventional step beer method.

[0038] The further conventional contact hole is filled up with a metal membrane, in order that an exposure development process may end by 1 time per one layer of wiring layers compared with the approach of covering and carrying out flattening of the substrate side by the insulating material afterwards, as a result of the number of wiring layers forming the multilayer interconnection whose number is five, a routing counter is reduced about 20% and the yield improves.

[0039] Compared with the embedding connection in the contact hole by the further conventional tungsten, connection resistance is falling to 3 by about 1/.

[0040] Thus, the multilayer interconnection obtained by the manufacture approach concerning this invention is a wiring consistency, a routing counter, and the thing that was extremely excellent in the field of an electrical property.

[0041] In addition, in said 2nd example, if the titanium film 5 as refractory metal film and the copper film 6 as plating cathode are formed after spreading of the photosensitive polyimide as plating resist, the photosensitive polyimide as plating resist can be used as an interlayer insulation film as it is, and a man day will be reduced sharply. By this approach explained as the 3rd example of this invention, this approach In advance of formation of the titanium film 5 which is refractory metal film, and the copper film 6 as plating cathode, so that the reverse pattern of the 2nd-layer wiring may be drawn The resist pattern 10 is formed and pattern plating is performed, and the whole surface is lightly etched after plating, and he removes the titanium film 5 and copper film 6 on a resist pattern 10, and is trying to use a resist pattern 10 as an interlayer insulation film as it is.

[0042] That is, it carries out like [formation (drawing 1 (a)) of a contact hole 9] said 1st

example, and then is drawing 4 (a). The photosensitive polyimide by Toray Industries, Inc. by which the designation is carried out to UR-3140 so that it may be shown is applied with a spin coat method, and it is 20 micrometers of thickness. An insulating layer is formed. Opening of the circuit pattern of the 2nd wiring layer is carried out by this postexposure development, and a resist pattern 10 is obtained. And 400 degrees C and heat treatment for 30 minutes are performed, and, subsequently the titanium film 5 which is refractory metal film, and the copper film 6 as plating cathode are formed by the sputtering method.

[0043] Then, it installs in plating equipment like said 2nd example, galvanizes on the same conditions, and is drawing 4 (b). It is 25 micrometers of thickness so that it may be shown. The copper-plating film 7 of extent is formed.

[0044] Next drawing 4 (c) It etches lightly with the mixed solution which consists of ammonium persulfate, a sulfuric acid, and ethanol, and it etches by Fukashi into whom the copper film 6 used among copper-plating film as copper films other than the circuit pattern of the 2nd wiring layer, i.e., plating cathode on the front face of a substrate, is etched, and the titanium film 5 is made to expose so that it may be shown. And etching removal of the titanium film 5 which is refractory metal film on substrate 1 principal plane is further carried out with the etching reagent which consists of EDTA, ammonia, and hydrogen peroxide solution.

[0045] thus, a multilayer interconnection with a flat substrate front face -- very -- **** -- it is formed easily.

[0046] According to this approach, compared with said 2nd example, a man day is reduced sharply.

[0047]

[Effect of the Invention] As explained above, according to this invention, there are few man days, and it becomes possible to obtain the small multilayer interconnection of a dimension conversion error.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The production process Fig. of the multilayer interconnection of the 1st example of this invention
[Drawing 2] Drawing showing the plating equipment used at this process
[Drawing 3] The production process Fig. of the multilayer interconnection of the 2nd example of this invention
[Drawing 4] The production process Fig. of the multilayer interconnection of the 3rd example of this invention
[Drawing 5] The production process Fig. of the multilayer interconnection of the conventional example
[Drawing 6] Drawing showing a multilayer-interconnection substrate
[Description of Notations]
1 Substrate
2 Insulator Layer
3 1st Wiring Layer
4 Interlayer Insulation Film
5 Titanium Film
6 Copper Film (Plating Cathode)
7 Copper-Plating Film
8 2nd Wiring Layer
9 Contact Hole
10 Resist Pattern

[Translation done.]

* NOTICES *

CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law
[Section partition] The 2nd partition of the 7th section
[Publication date] July 27, Heisei 13 (2001. 7.27)

[Publication No.] JP,7-58201,A
[Date of Publication] March 3, Heisei 7 (1995. 3.3)
[Annual volume number] Open patent official report 7-583
[Application number] Japanese Patent Application No. 5-202330
[The 7th edition of International Patent Classification]

H01L 21/768
21/3205

[FI]

H01L 21/90 A
21/88 K

[Procedure revision]
[Filing Date] August 14, Heisei 12 (2000. 8.14)
[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] The name of invention
[Method of Amendment] Modification
[Proposed Amendment]
[Title of the Invention] The manufacture approach of a multilayer-interconnection substrate and multilayer-interconnection equipment
[Procedure amendment 2]
[Document to be Amended] Specification
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[Proposed Amendment]
[Claim(s)]
[Claim 1] The process of the interlayer insulation film which has the side-attachment-wall section which constitutes the crevice for an interlayer connection which forms the electrode for electroplating in said side-attachment-wall section at least,
The manufacture approach of the multilayer-interconnection equipment characterized by providing the process which fills said crevice with this plating film while forming the plating film by electroplating on this electrode.
[Claim 2] The manufacture approach of the multilayer-interconnection equipment according to claim 1 characterized by constituting the plating film from copper or a copper alloy.

[Claim 3] The manufacture approach of the multilayer-interconnection equipment according to claim 1 characterized by forming the electrode which has the operation which prevents diffusion of the oxygen from an interlayer insulation film to the plating film, and electroplating copper or a copper alloy using this electrode.
[Claim 4] The manufacture approach of the multilayer-interconnection equipment according to claim 1 characterized by forming an electrode equipped with the film which consists of the copper or the copper alloy formed in the barrier which prevents the counter diffusion of an interlayer insulation film and the plating film, and this barrier front face, and electroplating copper or a copper alloy using this electrode.
[Claim 5] The barrier is the manufacture approach of the multilayer-interconnection equipment according to claim 4 characterized by forming by vacuum evaporationo or sputtering among a tantalum, titanium, nickel, vanadium, niobium, chromium, molybdenum, and a tungsten using a kind at least.
[Claim 6] The manufacture approach of the multilayer-interconnection equipment according to claim 1 characterized by adding the organic substance with which the deposit rate of the plating film in a crevice becomes the plating bath used for electroplating early as compared with other fields.
[Claim 7] The manufacture approach of the multilayer-interconnection equipment according to claim 1 characterized by a kind being suitably added at least among organic nitrogen compounds, an organosulfur compound, or a polyether compound by the plating bath used for electroplating.
[Claim 8] The process which forms the interlayer insulation film which has the side-attachment-wall section which constitutes the crevice for an interlayer connection on the 1st wiring layer,
The process which forms the electrode for electroplating in said side-attachment-wall section at least, and forms the plating film on said electrode by electroplating,
The process which removes said plating film and said electrode on said front face of an interlayer insulation film so that said plating film in said crevice may be made to remain,
The process which forms the 2nd wiring layer in said interlayer insulation film front face so that said plating film may be contacted,
The manufacture approach of the multilayer-interconnection substrate characterized by providing.
[Claim 9] The process which forms the interlayer insulation film which has the side-attachment-wall section which constitutes the crevice for an interlayer connection on the 1st wiring layer,
The process which forms the electrode for electroplating in said interlayer insulation film front face which contains said side-attachment-wall section at least,
The process which arranges the mask of a predetermined pattern on said electrode,
The process which forms the plating film on said electrode by electroplating using said electrode,

The manufacture approach of the multilayer-interconnection substrate characterized by providing the process which removes said electrode of Hazama of a mask, and said this mask and said interlayer insulation film, and forms an insulator layer further on this removed predetermined pattern.
[Claim 10] The process which forms the interlayer insulation film which has a thick part by the pattern which reversed the 2nd wiring layer while having the side-attachment-wall section which constitutes the crevice for an interlayer connection on the 1st wiring layer,
The process which forms the electrode for electroplating on said interlayer insulation film,
The manufacture approach of the multilayer-interconnection substrate characterized by providing the process which forms the plating film on said electrode by electroplating on said electrode.
[Procedure amendment 3]
[Document to be Amended] Specification
[Item(s) to be Amended] 0012
[Method of Amendment] Modification
[Proposed Amendment]
[0012] In the 1st of this invention, the process of the interlayer insulation film which has the

side-attachment-wall section which constitutes the crevice for an interlayer connection in the manufacture approach of multilayer-interconnection equipment which forms the electrode for electroplating in said side-attachment-wall section at least, and the process which fills said crevice with this plating film while forming the plating film by electroplating on this electrode are provided. Moreover, the oxidation silicone film formed by the polyimide resin, the applying method, the chemical vapor deposition, or the sputtering method formed by the applying method is used for said insulator layer. In addition, the organic nitrogen compounds which are added during a plating bath and to add, an organosulfur compound, and a polyether compound are blended optimum dose every so that the level difference made on the plating film front face on opening formed in the insulating layer may become as small as possible.

[Procedure amendment 4]
[Document to be Amended] Specification
[Item(s) to be Amended] 0013
[Method of Amendment] Modification
[Proposed Amendment]
[0013] The process which forms the interlayer insulation film which has the side-attachment-wall section which constitutes the crevice for an interlayer connection on the 1st wiring layer in the manufacture approach of a multilayer-interconnection substrate in the 8th of this invention, The process which forms the electrode for electroplating in said side-attachment-wall section at least, and forms the plating film on said electrode by electroplating, The process which removes said plating film and said electrode on said front face of an interlayer insulation film so that said plating film in said crevice may be made to remain, and the process which forms the 2nd wiring layer in said interlayer insulation film front face so that said plating film may be contacted are provided.

[Procedure amendment 5]
[Document to be Amended] Specification
[Item(s) to be Amended] 0014
[Method of Amendment] Modification
[Proposed Amendment]
[0014] The process which forms the interlayer insulation film which has the side-attachment-wall section which constitutes the crevice for an interlayer connection on the 1st wiring layer in the manufacture approach of a multilayer-interconnection substrate in the 9th of this invention, The process which forms the electrode for electroplating in said interlayer insulation film front face which contains said side-attachment-wall section at least, The process which arranges the mask of a predetermined pattern on said electrode, and the process which forms the plating film on said electrode by electroplating using said electrode, Said electrode of Hazama of a mask, and said this mask and said interlayer insulation film is removed, and the process which forms an insulator layer further on this removed predetermined pattern is provided.

[Procedure amendment 6]
[Document to be Amended] Specification
[Item(s) to be Amended] 0015
[Method of Amendment] Modification
[Proposed Amendment]
[0015] The process which forms the interlayer insulation film which has a thick part by the pattern which reversed the 2nd wiring layer while having the side-attachment-wall section which constitutes the crevice for an interlayer connection from the 10th of this invention on the 1st wiring layer in the manufacture approach of a multilayer-interconnection substrate, the process which form the electrode for electroplating on said interlayer insulation film, and the process which form the plating film on said electrode by electroplating on said electrode provide.

[Translation done.]

MANUFACTURE OF MULTILAYER WIRING BOARD

Publication number: JP7058201
Publication date: 1995-03-03
Inventor: HIGUCHI KAZUTO; YAMADA HIROSHI; SAITO MASAYUKI
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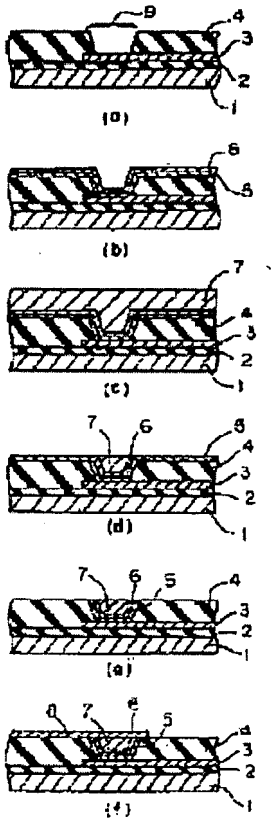
Classification:
- international: ***H01L21/3205; H01L21/768;*** *H05K3/40; H05K3/46;* **H01L21/02; H01L21/70;** H05K3/40; H05K3/46; (IPC1-7): H01L21/768; H01L21/3205
- European:
Application number: JP19930202330 19930816
Priority number(s): JP19930202330 19930816

Abstract of **JP7058201**

PURPOSE:To obtain a highly reliable multilayer wiring which can be brought into the state of high density easily by a method wherein, after a contact hole is formed in the insulating film of a board and flat surface is obtained by plating, a wiring layer is formed in such a manner that it is brought into contact with the flat surface. CONSTITUTION:A copper thin film pattern is formed on the insulating film 2 formed on the surface of a board 1 as the first layer wiring film 3. Photosensitive polyimide is coated thereon, and after a contact hole 9, with a side of about 20mum, has been formed by conducting an exposing and developing operation, a heat treatment is conducted at 400 deg.C for thirty minutes, and an interlayer insulating film 4 is formed. Then, after forming a titanium film 5 and a copper film 6 successively in 1mum thickness using a sputtering method, a thick copper- plating film 7 is formed on a recessed part by conducting electric plating under the condition wherein a flat surface can be obtained using the above-mentioned titanium film 5 and copper film 6 as an electrode. A titanium-copper-titanium multilayer thin film 8 is formed on the board 1 for which burying is conducted as the second wiring layer. As a result, a highly precise multilayer wiring can be obtained by reduced manhours.



(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平7－58201

(43)公開日　平成７年(1995)３月３日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｈ０１Ｌ　21/768					
21/3205					
		8826－4M	Ｈ０１Ｌ	21/ 90	Ａ
		8826－4M		21/ 88	Ｋ

審査請求　未請求　請求項の数２　ＯＬ　（全 ７ 頁）

(21)出願番号　特願平5－202330

(22)出願日　平成５年(1993)８月16日

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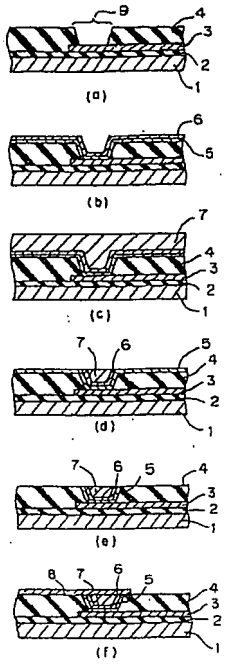
(54)【発明の名称】　多層配線基板の製造方法

(57)【要約】

【目的】　本発明は、高密度化が容易で信頼性の高い多層配線を提供することを目的とする。

【構成】　本発明では、基板上に形成された第１の配線層３上に層間絶縁膜４を形成し、これにコンタクトホール９を形成した後、基板表面全体を導電膜５，６で被覆し、この導電膜５，６を電極として、凹部に厚いめっき膜７が得られ、平坦な表面を得るような条件で電気めっきを行い、表面の平坦化を行った後、このめっき膜にコンタクトするように第２の配線層８を形成する。



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【特許請求の範囲】
【請求項１】　基板表面またはこの上層に形成された第１の配線層上に層間絶縁膜を形成し、これにコンタクトホールを形成する工程と、
前記基板表面全体を導電膜で被覆し、この導電膜を電極として、凹部に厚いめっき膜が得られるような条件下で電気めっきを行い表面を平坦化する工程と、
前記層間絶縁膜上のめっき膜を除去し前記コンタクトホール内のめっき膜を選択的に残留せしめるように前記めっき膜を等方エッチングする工程と、
このめっき膜にコンタクトするように第２の配線層を形成する工程とを含むことを特徴とする多層配線基板の製造方法。
【請求項２】　基板表面またはこの上層に形成された第１の配線層上に第１の層間絶縁膜を形成し、これにコンタクトホールを形成する工程と、
この上層に第２の絶縁膜を形成し、これをパターニングして、第２の配線層パターン形成領域を選択的に除去し凹部を形成する工程と、
前記基板表面全体を導電膜で被覆し、この導電膜を電極として、前記凹部に厚いめっき膜が形成されるような条件下で電気めっきを行い表面を平坦化する工程と、
前記第２の絶縁膜上のめっき膜を除去し前記凹部内のめっき膜を選択的に残留せしめるように前記めっき膜を等方エッチングする工程とを含むことを特徴とする多層配線基板の製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、多層配線基板の製造方法に係り、特に配線が高密度に形成された多層配線基板の製造方法に関する。
【０００２】
【従来の技術】近年、半導体集積回路技術の発達により電子機器の小型化、薄型化、高性能化が進められており、これに伴い回路基板上に半導体チップを高密度に実装することが重要な課題となっている。
【０００３】従って、多層配線基板内の配線も近年高密度化の方向にあり、配線の微細化、多層化が進んでいる。微細配線を形成するために従来は図５に示すように、基板１表面に絶縁層２を介して形成された薄膜金属層３からなる第１層配線上に、層間絶縁膜４を形成してこれにコンタクトホール９を形成し（図５(a)）、この後さらに薄膜金属層８を形成し（図５(b)）、レジストパターン１３（図５(c)）を介して、薄膜金属層８をエッチングし第２層配線のパターンを得る（図５(d)）という方法がとられている。
【０００４】しかしながらこの方法で多層配線を形成しようとすると、コンタクトホール９上の絶縁膜が凹状となっているため、さらにこの上に第２層配線と第３層配線を接続するためのコンタクトホールを形成するとコンタクトホールがいっそう深くなるため、配線の段切れが生じ易くなる。このため、図６に示すように３層以上の配線（３，８，１３）を形成する多層配線ではコンタクトホール９の位置をずらして設ける必要があり、結果的には配線密度の低下を招くことになる。

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【０００５】また、層間接続部を有する配線層材料としては、絶縁層との密着性、耐蝕性などの問題からアルミニウムや金が使用されてきたが、アルミニウムは抵抗が高く、金はコストが高いという問題があった。
【０００６】このため、配線層間の接続部分の上部が凹状とならないようにコンタクトホールに金属を埋め込むようにした接続法を用いる試みがなされている。例えば、図６に示すように、後に形成する絶縁層４と同程度の膜厚の金属膜をあらかじめ蒸着法あるいはスパッタリング法などによって形成しておくようにし、その上に塗布法により絶縁膜４を形成し表面を平坦化するという方法も提案されている。しかしながらこの方法では完全に平坦化するのは困難であり、金属膜が突出した形状になってしまい、後に形成するコンタクトホール周辺は他の部分より盛り上がってしまい、かえって逆効果になってしまう。
【０００７】また、この金属膜の材料としては特に限定はないが、低抵抗で低コストの層間接続を達成するために、銅や銅合金を用いる場合は、腐食防止と絶縁膜中への拡散を防止するためにこの金属膜形成後にこの上層を被覆保護する工程を設けなければならず、工数が増大するという問題がある。
【０００８】このような問題を解決するため、エッチング工程を必要としない方法として選択成長法があり、半導体チップの製造工程では実用化されている。この方法は、絶縁膜中に形成されたコンタクトホール底部に露出した配線部分のみに選択的にタングステンなどの金属を、化学的気相成長法により成長させ、平坦な層間接続部を得ようとするものである。しかしながら、この方法では使用する金属材料が化学的気相成長法および選択成長の可能な材料に限定される。現在、一般的に使用されている金属材料はタングステンであり、高融点材料で腐食されにくく、絶縁膜への拡散も少ないため、比較的使用し易い材料であるが、抵抗率が高くコンタクト抵抗を下げることが困難となっている。さらに化学的気相成長工程では基板温度が比較的高温となるため、絶縁膜としても耐熱性の高い材料が必要となり、誘電率が高く電気的特性に優れた有機絶縁膜では高温プロセスに絶えることができず必然的に使用不可能となってしまうという問題がある。
【０００９】
【発明が解決しようとする課題】このように、高密度配線を有する多層配線を実現するためには、コンタクトホールに金属が埋め込まれ平坦化された層間接続が必要となる。しかしながら、いずれの方法によっても、高密度

化に際して特性が良好で信頼性の高い多層配線を得ることができないという問題があった。

【００１０】本発明は前記実情に鑑みてなされたもので、高密度化が容易で信頼性の高い多層配線を提供することを目的とする。

【００１１】

【課題を解決するための手段】そこで本発明では、基板上に形成された第１の配線層上に層間絶縁膜を形成し、これにコンタクトホールを形成した後、基板表面全体を導電膜で被覆し、この導電膜を電極として、凹部に厚いめっき膜が形成され、平坦な表面を得るような条件で電気めっきを行い、表面の平坦化を行った後、このめっき膜にコンタクトするように第２の配線層を形成している。

【００１２】望ましくは、基板上に第１の配線層を形成する工程と、前記第１の配線層上に絶縁膜を形成しこれにコンタクトホールを形成する工程と、該コンタクトホールを形成した絶縁膜上に、銅または銅合金よりも融点の高い高融点金属層を含む薄膜導電層を形成する工程と、前記薄膜導電層上面に有機物を添加しためっき浴を用いて銅または銅合金よりも融点の高い高融点金属層を含む薄膜導電層を形成する工程と、前記薄膜導電層上面に有機物を添加しためっき浴を用いて銅または銅合金の電気めっきを行い基板主面上を前記めっき膜で平坦化する工程と、前記めっき膜を等方エッチングしてコンタクトホールに形成された銅または銅合金を前記絶縁膜と同じ厚みを残して基板主面上のめっき金属膜を除去する工程とを含むようにしている。

【００１３】また本発明の第２では、第１の層間絶縁膜にコンタクトホールを形成したのち薄膜導体層の形成に先立ち、第２の絶縁膜を形成し、これをパターニングして、第２の配線層パターン形成領域を選択的に除去して凹部を形成し、この後基板表面全体を導電膜で被覆し、この導電膜を電極として、凹部に厚いめっき膜が得られるような条件下で電気めっきを行い表面を平坦化し、前記第２の絶縁膜上のめっき膜を除去し前記凹部内のめっき膜を選択的に残留せしめるように前記めっき膜を等方エッチングするようにし、コンタクトホールに起因する凹部の埋め込みと第２の配線層の形成とを同時にめっきによって達成するようにしている。

【００１４】前記絶縁層としては、塗布法によって形成したポリイミド樹脂または塗布法あるいは化学的気相成長法あるいはスパッタリング法により形成した酸化シリコン膜等を用いる。さらに高融点金属としてはチタン、ニッケル、バナジウム、ニオブ、タンタル、クロム、モリブデン、タングステンの内少なくとも１種を用いるようにしている。これらは蒸着法あるいはスパッタリング法で形成する。

【００１５】なお、めっき浴中に添加する有機物としては有機窒素化合物、有機硫黄化合物、ポリエーテル化合物を絶縁層に形成された開口部上のめっき膜表面にできる段差ができるだけ小さくなるように適量づつ配合する。

【００１６】

【作用】上記方法によれば、例えば有機添加剤を用いためっき液の場合、凹部に厚いめっき膜が得られ、平坦な表面を得ることができる点に着目してなされたもので、絶縁膜にコンタクトホールを形成した後、めっきを行い平坦な基板表面を得たのち、このめっき膜を等方的にエッチングして、エッチングが絶縁膜の表面まで進行した時点で終了させれば、コンタクトホール内にのみ選択的にめっき膜が残され、埋め込みが完了する。このようにして、コンタクトホールの形成にのみ露光現像工程を用いるのみで、埋め込みが完了し、工数が少ない上、寸法の変換誤差が極めて小さくなる。

【００１７】ここで、電気めっきによる銅あるいは銅合金膜等の形成工程において、めっき浴には有機物を適量添加することにより、析出膜表面の平坦化を促進することができる。さらに好ましくはめっき工程中の陰極電流密度は析出金属膜に焦げが発生せず、かつ局部への電流集中による異常成長が起こらない範囲でなるべく高電流密度を用いるようにする。

【００１８】この工程において、コンタクトホールの形成後、チタン、ニッケル、バナジウム、ニオブ、タンタル、クロム、モリブデン、タングステンなどの高融点金属を電気めっきの陰極の一部として用いることにより、めっきによる銅あるいは銅合金は絶縁膜に直接触れることがなくなり、銅あるいは銅合金の腐食防止、絶縁膜への拡散防止をはかることができ、また絶縁膜との接着力を高めることができる。　さらに電気めっきによる金属膜の形成に際しては、有機窒素化合物、有機硫黄化合物、ポリエーテル化合物を適量添加することにより、凹凸のある表面に対しては凸部で凹部に比べて有機物が優先的に吸着するため、めっき膜の析出を抑制する。この結果凸部ではめっき膜の析出速度が遅くなり凹部では速くなるため、めっきを続行した場合、結果として表面の凹凸がなくない、表面が平坦化される。　このようにして形成された金属膜は、コンタクトホール部を除き、均一な膜厚となり、一方コンタクトホール部は他の部分に比べて厚くなる。従ってこの膜をエッチング速度が厚さ方向に均一であるようなエッチャントを用いてエッチングするようにすれば、コンタクトホール内部の銅あるいは銅合金を選択的に残し、他の部分の金属膜を除去することが可能となる。

【００１９】

【実施例】以下、本発明の実施例について図面を参照しつつ詳細に説明する。

【００２０】まず、基板１の表面に絶縁膜２を形成し、この上層に第１層配線膜３として銅薄膜パターンを形成し、この上層に、フォトニースＵＲ－３１４と指称され

ている東レ社製の感光性ポリイミドを塗布し、露光現像を行い、１辺２０μm 程度のコンタクトホール９を形成する。こののち、４００℃で３０分程度の熱処理を行い、層間絶縁膜４を形成する（図１(a)）。ここでポリイミドは熱処理後の膜厚が２０μm 程度となるように塗布時の膜厚を設定する。また段切れを防ぐため、コンタクトホールの底部と側壁との角度が１００度以上となるように露光現像条件をコントロールする。

【００２１】次いで、スパッタリング法によりチタン（Ｔｉ）膜５および銅（Ｃｕ）膜６を順次連続的に積層し、全体としての膜厚が１μm 程度となるようにする。ここで銅膜はめっき陰極として作用するものである。またチタンは高融点金属であり、層間絶縁膜であるポリイミドあるいは第１層配線である銅と、めっき陰極および上層のめっき膜とのとの相互拡散を防止するバリアとして作用する。従って膜厚は薄くて良い。銅とポリイミドが直接接するように形成されると、ポリイミド中の酸素によって銅が酸化され、密着性が低下し、剥離し易くなる。また連続的に形成するのはチタン表面が酸化されやすいためである。このように真空を破ることなく連続的に上層の膜を形成することにより、自然酸化膜が介在することなく低抵抗の膜が形成される。

【００２２】このようにして、基板１を図２に示すように電気めっき装置に設置し、この陰極にめっき陰極として銅膜６を接続する。ここでめっき浴としては、硫酸銅75g/l，硫酸（比重1.84）100ml/l からなる溶液にポリエチレングリコール100mg/lとチオ尿素10mg/lを添加したものを用い、液温を２５℃に設定して電流密度５A/dm^2 で撹拌しながらめっきを行い膜厚２０μm 程度の銅めっき膜７を形成する。コンタクトホールによる段差は１μm 程度であるため、２０μm 程度のめっき膜を形成するようにすれば十分に平坦な表面を得ることができる（図１(c)）。

【００２３】この後、図１(d) に示すように基板１表面に形成された銅めっき膜７を、過硫酸アンモニウム、硫酸、エタノールからなる混合溶液でエッチングし、基板表面の銅膜６（めっき陰極）も含めて除去し、コンタクトホール内にのみ残留せしめる。

【００２４】次いで、図１(e) に示すように，基板１主面上のチタン膜５をＥＤＴＡ、アンモニア、過酸化水素水からなるエッチング液でエッチング除去する。

【００２５】このようにして埋め込みを行った基板１に第２配線層としてチタン－銅－チタンの積層薄膜８を形成する（図１(f)）。

【００２６】ここで必要に応じて層間絶縁膜の形成から、この工程を繰り返し、多層配線を形成するようにしてもよい。

【００２７】このようにして、コンタクトホール９の形成に露光現像工程を用いるのみで、埋め込みが完了し、工数が少なく、寸法変換誤差が極めて小さく高精度の多層配線を行うことが可能となる。

【００２８】なお、前記実施例では、第１層配線と第２層配線とが直接接続された例について説明したが、第１層配線と第２層配線とが直接接続されず、間に１層または多層の他の配線層が介在し、間接的に第１層配線と第２層配線とが接続されるようにしてもよい。

【００２９】次に本発明の第２の実施例について説明するこの方法では、めっきに先立ち、第２層配線の反転パターンを描くようにレジストパターン１０を形成しておき、パターンめっきを行い、めっき後にレジストパターン１０を除去してできた凹部に塗布絶縁膜４を充填するようにし、コンタクトホールの埋め込みと第２配線層パターンの形成を同時に行うようにしたことを特徴とする。

【００３０】すなわち、めっき陰極の形成工程（図１(a) および図１(b)）までは前記第１の実施例と同様に行い、次に図３(a) に示すようにＡＺ－４９０３と指称されているヘキストジャパン社製の厚膜レジストを、スピンコート法により塗布して膜厚２５μm のめっきレジスト層を形成し９０℃でベーキングを行う。この後、露光現像により第２配線層の配線パターンを開口させ、レジストパターン１０を得る。

【００３１】次いで前記第１の実施例と同様にしてめっき装置に設置し、同様の条件でめっきを行い、図３(b) に示すように膜厚２０μm 程度の銅めっき膜７を形成する。この後図３(c) に示すようにレジストパターン１０をアセトンで除去し、銅めっきによって形成された第２配線層の配線パターン以外の銅膜すなわち基板表面のめっき陰極として用いた銅膜６を、過硫酸アンモニウム、硫酸、エタノールからなる混合溶液でエッチングする。さらに、この後基板１主面上のチタン膜５をＥＤＴＡ、アンモニア、過酸化水素水からなるエッチング液でエッチング除去する。

【００３２】この後第２配線層の形成されている基板表面に感光性ポリイミド（フォトニースＵＲ－３１４０）を塗布し、露光現像により、第２配線層上に形成されて突出している感光性ポリイミド４を除去する（図３(d)）。

【００３３】この後必要に応じて再度感光性ポリイミドを塗布すれば、さらに平坦な表面を得ることができる。

【００３４】このようにして容易に多層配線を得ることが可能となる。図３(d) の露光現像工程では、パターン精度はあまり必要でなく、ややずれが生じてもよい。

【００３５】また、図３(d) に示した露光現像工程は、十分に平坦化されて感光性ポリイミドが塗布されている場合は省略しても良く、この場合露光現像工程が完全に１回省略できることになる。

【００３６】また、さらに多層の配線を形成する場合は再度感光性ポリイミドを塗布し前述した工程を繰り返すようにすればよい。

【００３７】かかる方法によれば、表面の凹凸はコンタクトホールの深さに対して±５％以内に抑えることができ、層間絶縁膜の厚さを２０μｍもしくは３０μｍとした場合でも表面の凹凸は±５％以内に抑えることができる。これは従来のステップ・ビア法の場合、形成後の表面の凹凸の程度がコンタクトホールの深さに対して±２５％程度であったのに比べ、表面の凹凸が大幅に向上していることがわかる。また表面の凹凸の程度が大幅に減少した結果、３層以上の配線層を有する多層配線においてもコンタクトホールの位置をずらしたりする必要がなくなり、コンタクトホール上にコンタクトホールを設けることができ、従来のステップ・ビア法に比べ、配線密度が約２０％向上した。

【００３８】さらに従来のコンタクトホールに金属膜を充填し、後から絶縁材料で基板面を覆い平坦化する方法に比べ、露光現像工程が配線層１層あたり１回ですむため、配線層数が５層の多層配線を形成した結果、工程数が約２０％削減され歩留まりが向上する。

【００３９】さらに従来のタングステンによるコンタクトホール内の埋め込み接続に比べ接続抵抗は約１／３に低下している。

【００４０】このように本発明にかかる製造方法で得た多層配線は、配線密度、工程数、電気特性の面で極めて優れたものとなっている。

【００４１】なお、前記第２の実施例において、めっきレジストとしての感光性ポリイミドの塗布後に高融点金属膜としてのチタン膜５およびめっき陰極としての銅膜６を形成するようにすれば、めっきレジストとしての感光性ポリイミドをそのまま層間絶縁膜として利用でき、工数が大幅に低減される。この方法を、本発明の第３の実施例として説明するこの方法では、高融点金属膜であるチタン膜５およびめっき陰極としての銅膜６の形成に先立ち、第２層配線の反転パターンを描くように、レジストパターン１０を形成しておき、パターンめっきを行い、めっき後に全面を軽くエッチングしレジストパターン１０上のチタン膜５および銅膜６を除去し、レジストパターン１０はそのまま層間絶縁膜として利用するようにしている。

【００４２】すなわち、コンタクトホール９の形成（図１(a)）までは前記第１の実施例と同様に行い、次に図４(a)に示すようにＵＲ－３１４０と指称されている東レ社製の感光性ポリイミドをスピンコート法により塗布して膜厚２０μｍの絶縁層を形成する。この後露光現像により第２配線層の配線パターンを開口させ、レジストパターン１０を得る。そして４００℃，３０分の熱処理を行い、次いでスパッタリング法により高融点金属膜であるチタン膜５およびめっき陰極としての銅膜６を形成する。

【００４３】この後、前記第２の実施例と同様にしてめっき装置に設置し、同様の条件でめっきを行い、図４(b)に示すように、膜厚２５μｍ程度の銅めっき膜７を形成する。

【００４４】この後図４(c)に示すように、過硫酸アンモニウム、硫酸、エタノールからなる混合溶液で軽くエッチングし、銅めっき膜の内、第２配線層の配線パターン以外の銅膜すなわち基板表面のめっき陰極として用いた銅膜６がエッチングされる深さまでエッチングしチタン膜５を露呈せしめる。そしてさらに、基板１主面上の高融点金属膜であるチタン膜５をＥＤＴＡ、アンモニア、過酸化水素水からなるエッチング液でエッチング除去する。

【００４５】このようにして平坦な基板表面をもつ多層配線がきわめてめて容易に形成される。

【００４６】この方法によれば、前記第２の実施例に比べ工数が大幅に低減される。

【００４７】

【発明の効果】以上説明してきたように本発明によれば、工数が少なく、寸法変換誤差の小さい多層配線を得ることが可能となる。

【図面の簡単な説明】

【図１】本発明の第１の実施例の多層配線の製造工程図

【図２】同工程で用いられるめっき装置を示す図

【図３】本発明の第２の実施例の多層配線の製造工程図

【図４】本発明の第３の実施例の多層配線の製造工程図

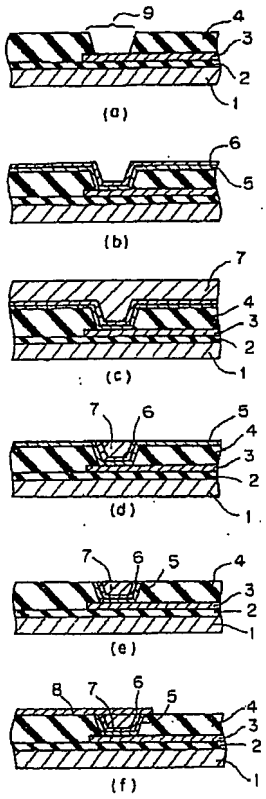
【図５】従来例の多層配線の製造工程図

【図６】多層配線基板を示す図

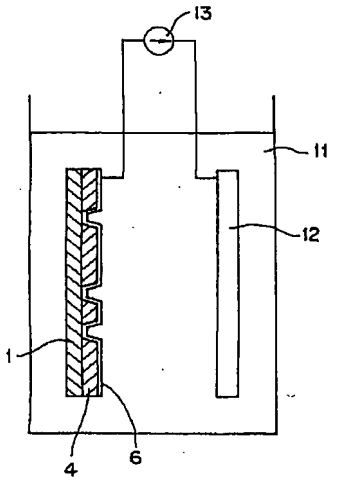
【符号の説明】

１　基板
２　絶縁膜
３　第１配線層
４　層間絶縁膜
５　チタン膜
６　銅膜（めっき陰極）
７　銅めっき膜
８　第２配線層
９　コンタクトホール
１０　レジストパターン

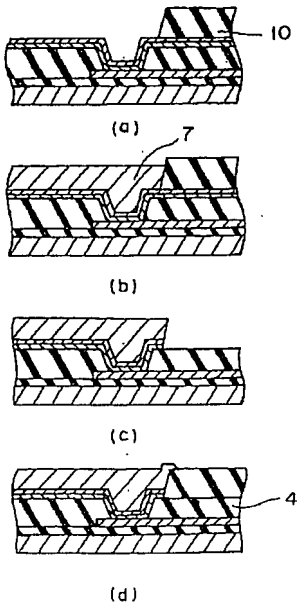
【図1】


9
4
3
2
1
(a)
6
5
(b)
7
4
3
2
1
(c)
7
6
5
4
3
2
1
(d)
7
6
5
4
3
2
1
(e)
8
7
6
5
4
3
2
1
(f)

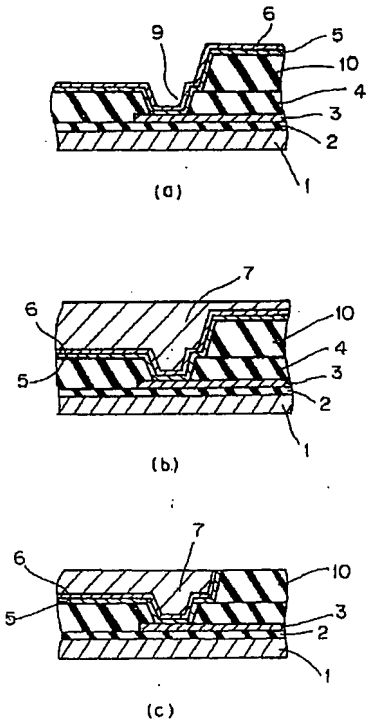
【図2】


13
11
12
1
4
6

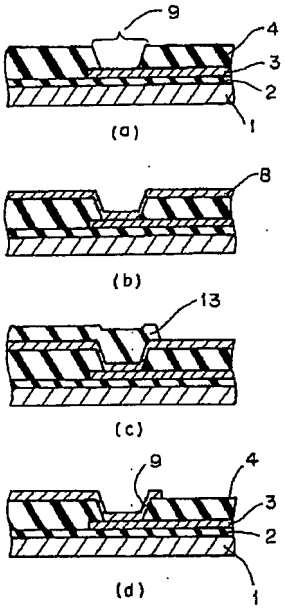
【図3】


10
(a)
7
(b)
(c)
4
(d)

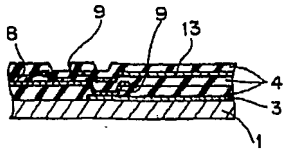
【図4】


9
6
5
10
4
3
2
1
(a)
7
6
10
4
5
3
2
1
(b)
7
6
10
5
3
2
1
(c)

【図5】



【図6】



【公報種別】特許法第１７条の２の規定による補正の掲載
【部門区分】第７部門第２区分
【発行日】平成１３年７月２７日（２００１．７．２７）

【公開番号】特開平７－５８２０１
【公開日】平成７年３月３日（１９９５．３．３）
【年通号数】公開特許公報７－５８３
【出願番号】特願平５－２０２３３０
【国際特許分類第７版】
H01L 21/768
21/3205
【ＦＩ】
H01L 21/90 A
21/88 K

【手続補正書】
【提出日】平成１２年８月１４日（２０００．８．１４）
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】発明の名称
【補正方法】変更
【補正内容】
【発明の名称】多層配線基板および多層配線装置の製造方法
【手続補正２】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】変更
【補正内容】
【特許請求の範囲】
【請求項１】　層間接続のための凹部を構成する側壁部を有する層間絶縁膜の少なくとも前記側壁部に電気めっきのための電極を形成する工程と、
この電極上に電気めっきによりめっき膜を形成するとともに、このめっき膜によって前記凹部を埋める工程とを具備することを特徴とする多層配線装置の製造方法。
【請求項２】　めっき膜を銅または銅合金で構成することを特徴とする請求項１記載の多層配線装置の製造方法。
【請求項３】　層間絶縁膜からめっき膜への酸素の拡散を防止する作用を有する電極を形成し、この電極を用いて銅または銅合金を電気めっきすることを特徴とする請求項１記載の多層配線装置の製造方法。
【請求項４】　層間絶縁膜とめっき膜との相互拡散を防止するバリアとこのバリア表面に形成される銅または銅合金からなる膜とを備える電極を形成し、この電極を用いて銅または銅合金を電気めっきすることを特徴とする請求項１記載の多層配線装置の製造方法。
【請求項５】　バリアは、タンタル、チタン、ニッケル、バナジウム、ニオブ、クロム、モリブデン、タングステンのうち、少なくとも一種を用いて、蒸着あるいはスパッタリングにより形成することを特徴とする請求項４記載の多層配線装置の製造方法。
【請求項６】　電気めっきに用いるめっき浴には、凹部におけるめっき膜の析出速度が他の領域に比して早くなる有機物が添加されていることを特徴とする請求項１記載の多層配線装置の製造方法。
【請求項７】　電気めっきに用いるめっき浴には、有機窒素化合物または有機硫黄化合物またはポリエーテル化合物のうち少なくとも一種が適宜添加されていることを特徴とする請求項１記載の多層配線装置の製造方法。
【請求項８】　第１の配線層上に層間接続のための凹部を構成する側壁部を有する層間絶縁膜を形成する工程と、
少なくとも前記側壁部に電気めっきのための電極を形成し、電気めっきにより前記電極上にめっき膜を形成する工程と、
前記凹部内の前記めっき膜を残留せしめるように前記層間絶縁膜表面の前記めっき膜および前記電極を除去する工程と、
前記めっき膜にコンタクトするように前記層間絶縁膜表面に第２の配線層を形成する工程と、
を具備することを特徴とする多層配線基板の製造方法。
【請求項９】　第１の配線層上に層間接続のための凹部を構成する側壁部を有する層間絶縁膜を形成する工程と、
少なくとも前記側壁部を含む前記層間絶縁膜表面に電気めっきのための電極を形成する工程と、
前記電極上に所定パターンのマスクを配設する工程と、
前記電極を用いて電気めっきすることにより前記電極上にめっき膜を形成する工程と、
前記マスクおよびこのマスクと前記層間絶縁膜との間の前記電極を除去し、この除去された所定パターン上にさ

らに絶縁膜を形成する工程とを具備することを特徴とする多層配線基板の製造方法。

【請求項１０】　第１の配線層上に層間接続のための凹部を構成する側壁部を有すると共に第２の配線層を反転したパターンで厚い部分を有する層間絶縁膜を形成する工程と、

前記層間絶縁膜上に電気めっきのための電極を形成する工程と、

前記電極上に電気めっきすることにより、前記電極上にめっき膜を形成する工程とを具備することを特徴とする多層配線基板の製造方法。

【手続補正３】

【補正対象書類名】明細書

【補正対象項目名】００１２

【補正方法】変更

【補正内容】

【００１２】本発明の第１では、多層配線装置の製造方法において、層間接続のための凹部を構成する側壁部を有する層間絶縁膜の少なくとも前記側壁部に電気めっきのための電極を形成する工程と、この電極上に電気めっきによりめっき膜を形成するとともに、このめっき膜によって前記凹部を埋める工程とを具備する。また、前記絶縁膜は、塗布法によって形成したポリイミド樹脂または塗布法あるいは化学的気相成長法あるいはスパッタリング法により形成した酸化シリコン膜等を用いる。なお、めっき浴中に添加する添加する有機窒素化合物、有機硫黄化合物、ポリエーテル化合物は、絶縁層に形成された開口部上のめっき膜表面にできる段差ができるだけ小さくなるように適量づつ配合する。

【手続補正４】

【補正対象書類名】明細書

【補正対象項目名】００１３

【補正方法】変更

【補正内容】

【００１３】本発明の第８では、多層配線基板の製造方法において、第１の配線層上に層間接続のための凹部を構成する側壁部を有する層間絶縁膜を形成する工程と、少なくとも前記側壁部に電気めっきのための電極を形成し、電気めっきにより前記電極上にめっき膜を形成する工程と、前記凹部内の前記めっき膜を残留せしめるように前記層間絶縁膜表面の前記めっき膜および前記電極を除去する工程と、前記めっき膜にコンタクトするように前記層間絶縁膜表面に第２の配線層を形成する工程とを具備する。

【手続補正５】

【補正対象書類名】明細書

【補正対象項目名】００１４

【補正方法】変更

【補正内容】

【００１４】本発明の第９では、多層配線基板の製造方法において、第１の配線層上に層間接続のための凹部を構成する側壁部を有する層間絶縁膜を形成する工程と、少なくとも前記側壁部を含む前記層間絶縁膜表面に電気めっきのための電極を形成する工程と、前記電極上に所定パターンのマスクを配設する工程と、前記電極を用いて電気めっきすることにより前記電極上にめっき膜を形成する工程と、前記マスクおよびこのマスクと前記層間絶縁膜との間の前記電極を除去し、この除去された所定パターン上にさらに絶縁膜を形成する工程とを具備する。

【手続補正６】

【補正対象書類名】明細書

【補正対象項目名】００１５

【補正方法】変更

【補正内容】

【００１５】本発明の第１０では、多層配線基板の製造方法において、第１の配線層上に層間接続のための凹部を構成する側壁部を有すると共に第２の配線層を反転したパターンで厚い部分を有する層間絶縁膜を形成する工程と、前記層間絶縁膜上に電気めっきのための電極を形成する工程と、前記電極上に電気めっきすることにより、前記電極上にめっき膜を形成する工程とを具備する。